Agenda

Rebaselining Review of the Run IIb

DZero Detector Project

November 5, 2003
Fermilab

- Introduction (Kotcher – 10')
- Trigger & DAQ/Online (Wood – 30')
  - AFE II/TriP (Bross – 15')
- BREAK
- Silicon Layer 0 (Lipton – 30')
- Baseline Change Proposal, Rebaseline Summary (Kotcher – 30')

Most everything you will see today is in draft form

Run IIb Project Organization
Nov '03

D0 Run IIb Project
J. Kotcher, Project Manager
V. O'Dell, Deputy (Trigger/DAQ); R. Lipton, Deputy (Silicon Layer 0)
W. Freeman, Associate, M. Johnson, Technical Coordinator
D. Knapp, Budget Officer; T. Erickson, Administration

WBS 1.1 Silicon ~~Terminated~~
M. Demarteau
G. Gaither

WBS 1.2 Trigger
P. Padley
D. Wood

- 1.2.1 L1 Cal Upgrade — M. Abolins, H. Evans
- 1.2.2 L1 Cal/Track Match — K. Johns
- 1.2.3 L1 Track Trigger — M. Narain
- 1.2.4 L2β Upgrade — R. Hirosky
- 1.2.5 Silicon Track Trigger — U. Heintz
- 1.2.6 Simulation — M. Hildreth
- 1.2.7 Administration (D. Wood)
- 1.2.8 AFE II/TriP — A. Bross, TBD

WBS 1.3 DAQ/Online
S. Fuess
P. Slattery

- 1.3.1 Level 3 Systems — D. Chapin, G. Watts
- 1.3.2 Network & Host Systems — J. Fitzmaurice, S. Krzywdzinski
- 1.3.3 Control Systems — F. Bartlett, G. Savage, V. Sirotenko
- 1.3.4 DAQ/Online Management (P. Slattery)

WBS 1.4 Project Administration

WBS 1.5 Installation
R. Smith

- 1.5.1 Silicon Installation — Mechanical: (W. Cooper) Electronics: L. Bagby
- 1.5.2 Trigger Installation — D. Edmunds

WBS 1.6 Silicon Layer 0
A. Bean
(R. Lipton)

- 1.6.1 Sensors — M. Demarteau, R. McCarthy
- 1.6.2 Readout Elec — A. Nomerotski, R. Sidwell
- 1.6.3 Mech Des & Fabrication — W. Cooper
- 1.6.4, 1.6.5 Detector Modules & Integ — J. Fast
- 1.6.6 Administration (A. Bean)

Installation an integrated part of project plan, but removed from formal Run IIb baselining

DZero Run IIb Rebaselining

- We will present today the scope, motivation, and status of the project we are proposing to rebaseline:
  - Status of ongoing, previously-baselined projects
    - Trigger (WBS 1.2)
    - DAQ/Online (WBS 1.3)
    - See talk by Wood
  - Silicon project costs to date; closeout costs
  - Approach to rebaselining: approach, what has been included
  - Motivation, technical approaches, and project plans for new sub-projects being put forward
    - Silicon Layer 0 (WBS 1.6) – see talk by Lipton
    - AFE II/TriP Upgrade (WBS 1.2.8) – see talk by Bross
    - Both are designed to enhance/maintain tracking capability in light of silicon cancellation
  - Discussion of backup documentation provided

Ongoing Projects

- All previously-approved trigger & DAQ/online sub-projects continue on as before
  - Technical progress excellent, commitment strong as ever, work continues unabated
  - These upgrades are dominated by university effort
  - Includes upgrade to Silicon Track Trigger (WBS 1.2.5), which is needed to accommodate layer 0
  - Cost of trigger project has increased, largely due to labor needs:
    - SACLAY dropped out (L1 Cal ADF) in response to silicon termination, effort was all in kind
    - Picked up by MSU, which must be supported through MIE funds
    - Other institutions (University of Illinois at Chicago, University of Virginia) are also contributing on smaller scale
    - $475k (unburdened FY02$) assumed for this in Draft Baseline Change Proposal submitted to DOE Oct 31
    - Estimate undergoing final evaluation

Silicon Layer 0
WBS 1.6

- While by no means a substitute for the upgraded Run IIb silicon, Layer 0 offers palpable improvements, provides a hedge against inner-layer radiation damage
  - Maintain pattern recognition, enhance impact parameter resolution
  - Technical issues resolved very quickly, project has rapidly coalesced
    - Draft Conceptual Design Report (144 pp), fully resource-loaded schedule in place
  - Critical mass of personnel assembled – interest is there, both Fermilab personnel and collaborating institutions, including silicon MRI institutions
- Single layer of silicon mounted on Run IIb beampipe, which is already in hand
  - Inserted into existing silicon through end calorimeter beampipe
  - Further discussion of technical details later today (Lipton)
- TPC of $2.6M includes ~ $650k in NSF MRI leftover funds from Run IIb silicon project
  - DOE MIE = $2.0M (includes contingency)

AFE II/TriP Upgrade
WBS 1.2.8

- We are proposing an upgrade to the Central Fiber Tracker (CFT) readout & triggering system
  - Maintain tracking capability in light of cancellation of silicon upgrade, particularly at increased luminosity
    - considerably improved noise performance – lower thresholds, enhance triggering, efficiency
    - z-information from timing
  - New Analog Front-End Boards (AFE II) and trigger (TriP) chip
    - First version TriP chip submitted with SVX4
    - Designed, tested by Fermilab (PPD, Yarema)
    - Was major success out of the box
    - First full AFE II prototype being laid out now, expect back by end CY03
    - System represents major simplification, performance upgrade
  - Exploiting considerable in-house experience – personnel, depth of technical knowledge
- TPC = $2.2M (includes 50% total contingency)
  - M&S cost estimate based on detailed past experience
  - see talk by Bross

Note on Installation

- Installation continues to undergo tremendous amount of scrutiny as project evolves
  - Installation schedule is very detailed, resource-loaded
- Layer 0 and trigger installation constantly reevaluated
  - Minimal interruption to complex and the acquisition of physics-quality luminosity
- Principals from the sub-projects themselves actively involved in developing project plan with WBS Level 2 manager
  - Also attracting new groups to take responsibility for installation, commissioning
- All major sub-projects, absent previous Run IIb silicon installation constraint, are converging on same time scale:
  - Ready for summer '05 shutdown
  - Duration 7 weeks (including Layer 0, Level 1 Calorimeter Trigger)
  - Other portions of trigger, DAQ/online can be installed earlier, adiabatically, and without Collision Hall access
- Although not formal part of rebaselined Run IIb project, two presentations on installation are provided in your documentation

Documentation Provided

- Plenary presentations
- Two presentations on Silicon Layer 0 installation
- Project schedules & milestones
- Basis of Estimate for Silicon Layer 0
- Responses to Oct 14 '03 Review of Layer 0
- Draft Layer 0 Conceptual Design Report
- Silicon Closeout Document
- Cost & Contingency Assessment
- Risk Analysis
- Draft Baseline Change Proposal, Change Controls
- Draft Addendum to Project Management Plan
- Draft Project Execution Plan